ABSTRACT OF THE DISCLOSURE

An SRAM memory cell is provided having a pair of cross-coupled CMOS inverters. The sources of the pull-up transistors forming each of the CMOS inverters are coupled to V_{CC} through parasitic resistance of the substrate in which each is formed. The source of the p-type pull-up transistor is therefore always at a potential less than or equal to the potential of the N-well such that the emitter-base junction of the parasitic PNP transistor cannot become forward biased and latch-up cannot occur.